

Appl. No. 10/749,103  
Reply to Office Action of June 30, 2005

Docket No. MIT-136BUS

Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of the claims in the application:

Please cancel Claims 1-27.

- 1 28. A method of providing a multi-layer semiconductor structure, the method  
2 comprising:  
3 providing a first semiconductor structure having first and second opposing  
4 surfaces; and  
5 disposing a laminate layer over a first one of the first and second opposing  
6 surfaces of the first semiconductor structure to provide a first semiconductor structure  
7 having a laminate layer disposed thereon.
- 1 29. The method of claim 28 further comprising:  
2 disposing a handle member over the laminate layer.
- 1 30. The method of claim 29 further comprising:  
2 a substrate on a second one of the first and second opposing surfaces of the first  
3 semiconductor structure.
- 1 31. The method of claim 30 further comprising:  
2 removing at least a portion of the substrate from the second one of the first and  
3 second opposing surfaces of the first semiconductor structure to provide a  
4 semiconductor-handle complex.
- 1 32. The method of claim 31 further comprising:  
2 providing a second semiconductor structure); and  
3 aligning a first surface of the semiconductor-handle complex with a first surface  
4 of the second semiconductor structure.

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- 1 33. The method of claim 32 further comprising:  
2 bonding the first surface of the second semiconductor structure to the first surface  
3 of the semiconductor -handle complex.
- 1 34. The method of claim 33 further comprising:  
2 removing the handle member and the laminate layer.
- 1 35. The method of claim 28 wherein providing a first semiconductor structure having  
2 first and second opposing surfaces comprises:  
3 a substrate having first and second opposing surfaces; and  
4 a first semiconductor structure over a first one of the first and second surfaces of  
5 the substrate.
- 1 36. The method of claim 28 wherein providing a first semiconductor structure having  
2 first and second opposing surfaces comprises:  
3 providing a semiconductor structure comprised of a plurality of thin film  
4 semiconductor layers.
- 1 37. The method of claim 29 wherein disposing a handle member over the laminate  
2 layer comprises:  
3 providing a handle substrate;  
4 disposing a film layer over at least one surface of the handle substrate.
- 1 38. The method of claim 37 wherein the film layer is provided from one of: silicon  
2 nitride; and silicon dioxide.
- 1 39. The method of claim 38 further comprising disposing a laminate over a surface of  
2 the handle member.
- 1 40. The method of claim 29 wherein disposing a handle member over the laminate  
2 layer comprises disposing a handle member over the laminate layer such that a surface of

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3 the laminate adheres to a surface of the handle member.

1 41. The method of claim 29 wherein disposing the laminate layer over a first one of  
2 the first and second opposing surfaces of the first semiconductor structure to provide a  
3 semiconductor structure having a laminate layer disposed thereon comprises providing a  
4 laminate layer comprised of a plurality of layers.

1 42. The method of claim 41 wherein providing a laminate layer comprised of a  
2 plurality of layers comprises:  
3 providing a first layer corresponding to a release layer;  
4 providing a second layer corresponding to a metal adhesion / diffusion barrier  
5 layer; and  
6 providing a third layer corresponding to a fusion layer.

1 43. The method of claim 42 wherein the release layer comprises at least one of  
2 zirconium and aluminum.

1 44. The method of claim 42 wherein the metal adhesion / diffusion barrier layer  
2 comprises tantalum.

1 45. The method of claim 42 wherein the fusion layer comprises at least one of copper,  
2 a polymer; and an inorganic dielectric.

1 46. The method of claim 41 wherein providing a laminate layer comprised of a  
2 plurality of layers comprises:  
3 providing a first layer corresponding to a metal adhesion / diffusion barrier layer;  
4 providing a second layer corresponding to a release layer; and  
5 providing a third layer corresponding to a fusion layer.

1 47. The method of claim 46 wherein the release layer comprises at least one of  
2 zirconium and aluminum.  
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1 48. The method of claim 46 wherein the metal adhesion / diffusion barrier layer  
2 comprises tantalum.

1 49. The method of claim 46 wherein the fusion layer comprises at least one of copper,  
2 a polymer, and an inorganic dielectric.

1 50. The method of claim 41 wherein providing a laminate layer comprised of a  
2 plurality of layers comprises providing a laminate layer comprised of two layers with a  
3 first one of the layers corresponding to a release layer and second one of the layers  
4 corresponding to one of:

5 a polymer having an adhesive characteristic which allows the laminate layer to  
6 adhere to the surface of the thin film semiconductor structure;  
7 an inorganic material; and  
8 copper.

1 51. The method of claim 28 wherein disposing a laminate layer comprises providing a  
2 laminate layer comprised of a single layer having an adhesive characteristic which allows  
3 the laminate layer to adhere to the surface of the semiconductor structure and having a  
4 characteristic such that the layer releases from the surface of the semiconductor structure  
5 in response to being exposed to a release agent.

1 52. The method of claim 29, wherein disposing a laminate layer comprises providing  
2 a laminate layer comprised of a single layer having an adhesive characteristic which  
3 allows the laminate layer to adhere to a surface of the handle member and having a  
4 characteristic such that the layer releases from the surface of the semiconductor structure  
5 in response to being exposed to a release agent.

1 53. The method of claim 31, wherein removing the substrate from the second one of  
2 the first and second opposing surfaces of the semiconductor structure to provide a  
3 semiconductor-handle complex comprises removing a portion of the second surface of

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4 the semiconductor-handle complex using at least one of: a mechanical grindback, an  
5 aqueous chemical etch; a vapor chemical etch; and a plasma etch.

1 54. The method of claim 33, wherein bonding the first surface of the second  
2 semiconductor structure to the first surface of the semiconductor-handle complex  
3 comprises providing bonding pads on at least one of the first surface of the second  
4 semiconductor structure; and the first surface of the semiconductor-handle complex.

1 55. The method of claim 54, wherein the bonding pads are provided from at least one  
2 of: copper; a polymer; and an inorganic dielectric.

1 56. The method of claim 34 wherein removing the handle member and the laminate  
2 layer comprises using at least one of:  
3 an aqueous-activated method;  
4 a vapor-activated method;  
5 a light-activated method;  
6 a temperature-activated method;  
7 an ion bombardment-activated method;  
8 an electrically-assisted method; and  
9 a mechanical method.

1 57. The method of claim 28 wherein the semiconductor structure corresponds to a  
2 die-to-die semiconductor structure.

1 58. The method of claim 28 wherein the semiconductor structure corresponds to a  
2 die-to-wafer semiconductor structure.

1 59. The method of claim 28 wherein the semiconductor structure corresponds to a  
2 wafer-to-wafer semiconductor structure.

1 60. The method of claim 28 wherein:  
2 providing a first semiconductor structure having first and second opposing

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3 surfaces comprises providing a first semiconductor structure having a face surface and a  
4 backside surface; and  
5 disposing a laminate layer comprises disposing a laminate layer over the face of  
6 the first semiconductor structure to provide a semiconductor structure having a laminate  
7 layer disposed thereon.

1 61. The method of claim 32 wherein:  
2 providing a second semiconductor structure comprises providing a second thin  
3 film semiconductor structure; and  
4 aligning a first surface of the semiconductor-handle complex with a first surface  
5 of the second semiconductor structure comprises aligning the backside of the  
6 semiconductor-handle complex with a face of the second thin film semiconductor  
7 structure.

1 62. The method of claim 1 wherein:  
2 the first semiconductor structure corresponds to an original semiconductor  
3 substrate;  
4 the first semiconductor-handle complex having a substrate portion corresponds to  
5 an original-handle complex having a substrate portion;  
6 the handle-semiconductor complex corresponds to a handle-thin film complex;  
7 the second semiconductor structure corresponds to a second substrate.

1 63. The method of claim 62 wherein:  
2 the original semiconductor substrate corresponds to a first thin-film substrate  
3 the second substrate corresponds to a second thin-film substrate.

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Please add the following new claims.

1 64. A multi-layer semiconductor structure comprising:  
2 a first semiconductor structure having first and second opposing surfaces; and  
3 a laminate layer over a first one of the first and second opposing surfaces of the

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4 first semiconductor structure to provide a first semiconductor structure having a laminate  
5 layer disposed thereon.

1 65. The structure of claim 64 further comprising a handle member disposed over the  
2 laminate layer.

1 66. The structure of claim 64 further comprising a substrate disposed on a second one  
2 of the first and second opposing surfaces of the first semiconductor structure.

1 67. The structure of claim 64 wherein the first semiconductor structure comprises a  
2 plurality of thin film semiconductor layers.

1 68. The structure of claim 65 further comprising a film layer disposed over at least  
2 one surface of the handle member.

1 69. The structure of claim 68 wherein the film layer is provided from one of: silicon  
2 nitride; and silicon dioxide.

1 70. The structure of claim 68 further comprising a laminate disposed over a surface of  
2 the handle member.

1 71. The structure of claim 64 wherein said laminate layer comprises:  
2 a first layer corresponding to a release layer;  
3 a second layer corresponding to a metal adhesion / diffusion barrier layer; and  
4 a third layer corresponding to a fusion layer.

1 72. The structure of claim 71 wherein the release layer comprises at least one of  
2 zirconium and aluminum.

1 73. The structure of claim 72 wherein the metal adhesion / diffusion barrier layer  
2 comprises tantalum.

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1 74. The structure of claim 73 wherein the fusion layer comprises at least one of  
2 copper; a polymer; and an inorganic dielectric.

1 75. The structure of claim 64 wherein said laminate layer comprises:  
2 a first layer corresponding to a metal adhesion / diffusion barrier layer;  
3 a second layer corresponding to a release layer; and  
4 a third layer corresponding to a fusion layer.

76. The structure of claim 75 wherein the release layer comprises at least one of  
zirconium and aluminum.

1  
1 77. The structure of claim 76 wherein the metal adhesion / diffusion barrier layer  
2 comprises tantalum.

1 78. The structure of claim 77 wherein the fusion layer comprises at least one of  
2 copper; a polymer; and an inorganic dielectric.

1 79. The structure of claim 64 wherein said laminate layer comprises two layers with a  
2 first one of the layers corresponding to a release layer and second one of the layers  
3 corresponding to one of:  
4 a polymer having an adhesive characteristic which allows the laminate layer to  
5 adhere to the surface of the thin film semiconductor structure;  
6 an inorganic material; and  
7 copper.

1 80. The structure of claim 64 wherein said laminate layer comprises a single layer  
2 having an adhesive characteristic which allows the laminate layer to adhere to the surface  
3 of the semiconductor structure and having a characteristic such that the layer releases  
4 from the surface of the semiconductor structure in response to being exposed to a release  
5 agent.

1 81. The structure of claim 64 wherein the semiconductor structure corresponds to a



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2 die-to-die semiconductor structure.

1 82. The structure of claim 64 wherein the semiconductor structure corresponds to a  
2 die-to-wafer semiconductor structure.

1 83. The structure of claim 64 wherein the semiconductor structure corresponds to a  
2 wafer-to-wafer semiconductor structure.

1 84. The structure of claim 64 wherein a portion of the substrate from the second one  
2 of the first and second opposing surfaces of the first semiconductor structure and the  
3 handle member provide a semiconductor-handle complex and wherein the structure  
4 further comprises:

5 a second semiconductor structure corresponding to a second thin film  
6 semiconductor structure disposed over a first surface of the semiconductor-handle  
7 complex with a first surface of the second thin film semiconductor structure aligned with  
8 a backside of the semiconductor-handle complex.

1 85. The structure of claim 84 wherein:

2 the first semiconductor structure corresponds to an original semiconductor  
3 substrate;

4 the first semiconductor-handle complex having a substrate portion corresponds to  
5 an original-handle complex having a substrate portion;

6 the handle-semiconductor complex corresponds to a handle-thin film complex;

7 and

8 the second semiconductor structure corresponds to a second substrate.

1 86. The structure of claim 85 wherein the original semiconductor substrate  
2 corresponds to a first thin-film substrate.

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